

**OLLSCOIL NA hEIREANN, CORCAIGH**  
**THE NATIONAL UNIVERSITY OF IRELAND, CORK**

**COLAISTE NA hOLLSCOILE, CORCAIGH**  
**UNIVERSITY COLLEGE, CORK**

**Summer Examinations 2012**

**CS4403 Introduction to Embedded Systems**

**Professor I. Gent**  
**Professor J. Bowen**  
**Dr J. G. Vaughan**

**Total Marks: 80**

**Answer TWO QUESTIONS**

**TIME ALLOWED: 1.5 hours**

**NO Calculators allowed**

### QUESTION 1 (40 Marks)

Consider the simple RISC processor architecture described in this module.

- (a) Give the formats of the three instruction types. **6 Marks**
- (b) List the five phases of instruction execution. **5 Marks**
- (c) Allowing for occasional slow memory access due to a cache miss, give the sequence of actions needed to fetch and execute the instruction

Load R5, X(R7)

**13 Marks**

- (d) Sketch the datapath for this machine and indicate where each of the stages 2 to 5 is located. **16 Marks**

### QUESTION 2 (40 Marks)

Consider the 5-stage pipelined RISC processor architecture described in this module.

- (a) Show how data dependencies in the following execution sequence are adequately assimilated using a pipeline stall.

Add R2, R3, #100

Subtract R9, R2, #30

**12 Marks**

- (b) Show how operand forwarding avoids the need for a stall in the case of the instructions shown in part (a). Sketch the architectural modifications needed to accommodate operand forwarding. **16 Marks**

- (c) Assume that memory access takes 3 clock cycles on a cache miss and 1 clock cycle on a hit. Show how, when a cache miss occurs, the instruction Load R2, (R3) creates memory delays for subsequent instructions in the absence of data dependencies. Show how, even with a cache hit, the following sequence may also cause a memory delay.

Load R2, (R3)

Subtract R9, R2, #30

**12 Marks**

**QUESTION 3 (40 Marks)**

- (a) Draw a block diagram of a typical microcontroller. Sketch the receive and transmit structure of a serial interface. In a separate diagram, show the registers that you would expect to find in a typical serial interface, labelling important bits appropriately. **15 Marks**
- (b) Give the salient characteristics of the Altera Nios II processor. List the Nios II addressing modes, specifying how they operate. What are the three Nios II instruction formats? **15 Marks**
- (c) Give at least five points relating to FPGA devices and their use in embedded systems. How is the Nios II processor specified? Summarize the operation of the Nios II interval timer. **10 Marks**